LO Calorimeter Trigger
LHCb Bologna

U. Marconi
INFN Sezione di Bologna

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Outline

- Introduction
- Status of the Selection Boards
- Optical Transmitters
- Plans
- Requests
LO Calorimeter Trigger

- Detect a local high $E_T$ cluster in ECAL or HCAL
  - 2x2 cells
    - From 8x8 cm$^2$ (Inner ECAL) to 52x52 cm$^2$ (Outer HCAL)
  - ECAL: 5952 cells $\rightarrow$ 5952 possible clusters
    - Validation by PS/SPD (same geometry) to get electron and photon candidates
    - Combination to get $p^0$ candidates.
  - HCAL: 1484 cells $\rightarrow$ 1484 possible clusters
    - Add the ECAL $E_T$ in front if available
The Selection Crate

- Data input @ 40 MHz
  - 28 electron clusters
  - 28 photon clusters
  - 2x28 neutral pion clusters (local, global)
  - 80 hadron clusters
  - 16 SPD hits partial sums
- Data output to the LODU @40MHz
  - Highest transverse energy clusters for each cluster type (5 highest)
  - Total transverse hadron energy (global trigger variable)
  - Total SPD hit multiplicity (global trigger variable)
- Data output to the L1 trigger @1.1MHz
  - The entire set of the processed clusters
Selection Board
(Select 1\textsuperscript{st} and 2\textsuperscript{nd} highest)

12 channel optical transducer

10-ch

Deserialization
Demu 2:1
Synchronization

8-ch

Deserialization
Demu 2:1
Synchronization

10-ch

Deserialization
Demu 2:1
Synchronization

TTCrq

Processing Unit
1200pins

Ghosts removal to select the 2nd highest

1-ch Tx

1-ch Tx

1-ch Tx

Glue Card

CCPC

ECS

Fast Control

Bus adapter: PCI to JTAG and I\textsuperscript{2}C
Selection Board
(Select 1\textsuperscript{st} highest)

12 channel optical transducer

10-ch

Deserialization Demu 2:1 Synchronization

Deserialization Demu 2:1 Synchronization

Deserialization Demu 2:1 Synchronization

10-ch

10-ch

8-ch

8-ch

L1 buffer

Processing Unit

TTCrq

Glue Card

CCPC

28 clusters of 32 bits to L1 in case of L0 accept

Fast Control

Highest and transverse energy sum

To the L0DU

1-ch Tx

1-ch Tx

1-ch Tx

1-ch Tx
Selection Board Test Setup

Optical Fiber Links

Pattern Generator

Selection Board Prototype
**BER measurements**

<table>
<thead>
<tr>
<th>BER</th>
<th>n(bits)</th>
<th>Δt</th>
</tr>
</thead>
<tbody>
<tr>
<td>$10^{-12}$</td>
<td>$2.3 \cdot 10^{12}$</td>
<td>30 min</td>
</tr>
<tr>
<td>$10^{-13}$</td>
<td>$2.3 \cdot 10^{13}$</td>
<td>5 h</td>
</tr>
<tr>
<td>$10^{-14}$</td>
<td>$2.3 \cdot 10^{14}$</td>
<td>50 h</td>
</tr>
</tbody>
</table>

Time of Measurements
When no error are detected
C.L. 90%

**Diagram:**
- **Pattern Generator**
  - VME Control
  - Xilinx FPGA
  - DG2040 Tektronix 40MHz
- **Transmitter boards**
- **Fiber Optical 1.6 Gb/s**
- **Receiver boards**
- **80 meters**
- **Crystal Oscillator 80MHz**
- **SDA 5000 Lecroy**
### Eye Diagram Technique

<table>
<thead>
<tr>
<th>Limit</th>
<th>Proportion of Population Within Limits</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>±1σ</td>
<td>68.2689%</td>
<td>0.16</td>
</tr>
<tr>
<td>±2σ</td>
<td>95.45%</td>
<td>$2.28 \times 10^{-2}$</td>
</tr>
<tr>
<td>±3σ</td>
<td>99.73%</td>
<td>$1.35 \times 10^{-3}$</td>
</tr>
<tr>
<td>±4σ</td>
<td>99.99367%</td>
<td>$0.32 \times 10^{-4}$</td>
</tr>
<tr>
<td>±5σ</td>
<td>99.9999427%</td>
<td>$2.87 \times 10^{-7}$</td>
</tr>
<tr>
<td>±6σ</td>
<td>100-1.973 x $10^{-7}$%</td>
<td>$0.98 \times 10^{-9}$</td>
</tr>
<tr>
<td>±7σ</td>
<td>100-2.5596 x $10^{-10}$%</td>
<td>$1.28 \times 10^{-12}$</td>
</tr>
<tr>
<td>±8σ</td>
<td>100-1.24419 x $10^{-13}$%</td>
<td>$0.62 \times 10^{-15}$</td>
</tr>
<tr>
<td>±9σ</td>
<td>100-2.25718 x $10^{-17}$%</td>
<td>$1.13 \times 10^{-19}$</td>
</tr>
<tr>
<td>±10σ</td>
<td>100-1.53398 x $10^{-21}$%</td>
<td>$0.77 \times 10^{-23}$</td>
</tr>
</tbody>
</table>
Input stage: 1/3 of the final 9U board at the actual component density.
Pattern Generator (BERT)

Single Channel Optical Tx Prototypes

Optical Transducer
Test of the ECS (slow control)

Test using the Linux OS

Credit Card PC

Genova test board

Glue Card
Optical Transmitters
Mezzanine Boards

<table>
<thead>
<tr>
<th>Board Type</th>
<th>Items</th>
<th>Spares</th>
<th>Plugged to</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-channel</td>
<td>16</td>
<td>4</td>
<td>PreShower&amp;SPD</td>
</tr>
<tr>
<td>1-channel</td>
<td>24</td>
<td>4</td>
<td>Selection Board</td>
</tr>
<tr>
<td>5-channels</td>
<td>18</td>
<td>4</td>
<td>CROC</td>
</tr>
<tr>
<td>8-channels</td>
<td>28</td>
<td>4</td>
<td>Validation Card</td>
</tr>
<tr>
<td>12-channels</td>
<td>26</td>
<td>4</td>
<td>CROC</td>
</tr>
</tbody>
</table>

Items: 112+20 boards
Single Channel Optical Transmitter (top side)

Control Status LED

Voltage-Optical Transducer

Vertical Cavity Surface Emitting Laser, made by ULM Photonics type ULM850-05-TN-USMB0P. High speed up to 5 Gbps. SMA fibre connector. Operate on multimode fibre at wavelength of 850nm.

Gigabit Optical Link, chip made by the CERN microelectronic group. It has been designed to be less sensitive to radiation effects.
Single Transmitter (bottom side)

Dip switch to set the GOL $I^2C$ address

SAMTEC High Speed Connectors 0.635mm Hi-Speed Header QTS and QSS series
Multichannel Optical Transmitter

- I2C addresses
- Clock distributor
- 250 pin/connector
- GOL
- Top side
- Optical Transducer: HFBR772BH
- Bottom side
Transmitter Test Board

- TTCrq
- Filtered Clock
- QPLL

External Clock
Pattern Generator

12 channels test platform

1 Channel test platform

Single Channel Tx

32 bits @ 40 MHz
MECHANICAL SPECIFICATIONS
Mezzanine Board - Single CH

Single channel optical link
Mechanical Specification

Multiple channels optical link
Plans

- **December 2004**: Test of the Optical Transmitters and test of the final prototype of the Selection Board
- **May–June 2005**: Purchasing of the fundamental electronics components (GOLs, Laser Diodes, etc) and of the optical fibers and of the optical patch panel
- **December 2005**: Building of the optical transmitters and the selection board
## Electronics Components

<table>
<thead>
<tr>
<th>Component</th>
<th>Vendor</th>
<th>Items</th>
</tr>
</thead>
<tbody>
<tr>
<td>GOL</td>
<td>CERN</td>
<td>800</td>
</tr>
<tr>
<td>1ch Laser Diode</td>
<td>ULM Photonics/CERN</td>
<td>60</td>
</tr>
<tr>
<td>12 ch Opt. Transd. Tx</td>
<td>Italy</td>
<td>30</td>
</tr>
<tr>
<td>12 ch Opt. Transd. Rx</td>
<td>Italy</td>
<td>40</td>
</tr>
<tr>
<td>TTCrq</td>
<td>CERN</td>
<td>12</td>
</tr>
<tr>
<td>Credit Card PC</td>
<td>CERN</td>
<td>12</td>
</tr>
<tr>
<td>Glue Card</td>
<td>CERN</td>
<td>12</td>
</tr>
</tbody>
</table>
### 2005 requests for fundings

<table>
<thead>
<tr>
<th>Description</th>
<th>Amount</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trasferte interne</td>
<td>10.0 KEuro</td>
</tr>
<tr>
<td>Trasferte estero</td>
<td>70.0 KEuro</td>
</tr>
<tr>
<td>Consumo e metabolismo</td>
<td>(5.0 + 10.0) KEuro</td>
</tr>
<tr>
<td>Inventariabile</td>
<td>5.0 KEuro</td>
</tr>
<tr>
<td>Costruzione apparati</td>
<td>300. KEuro</td>
</tr>
</tbody>
</table>
The Selection Board

Input Interface

Processing Unit

Inter-Board Communications

Demultiplexers 28

Deserializers 28x16 = 448 bits

10 lines differential

Optical Rx Transducer

8 lines differential

Optical Rx Transducer

Optical Rx Transducer

10 lines differential

TLK2501

Demultiplexer

Demultiplexer

Demultiplexer

Demultiplexer

Demultiplexer

Demultiplexer Alignement

28x24 bits

2x44 bits

44 bits

Serializer GOL

32 bits

Serializer GOL

QPLL

32x32 bits

TTCrx

46 bits

Clock

Ethernet

Clock

7 bits

ECS

Output Interface

2x32 bits

Optical Tx Transducer

L0DU or Hadron Master

TELL1

44 bits

OpticalTx Trasducer

Input Interface Processing Unit

Output Interface

Slow Control

Fast Control