SpaceWire IP Cores for High Data Rate and Fault Tolerant Networking

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Outline

- Overview of SpaceWire standard
- SpaceWire Intellectual Property Cores
  - Interface
  - Router
- Prototyping Environment
SpaceWire Overview (1/2)

- SpaceWire basics:
  - European Space Agency
  - Serial, Full-Duplex links
  - Distances: 10-20 meters
  - LVDS data/strobe signals
  - High rate (2-400 Mbps)
  - Point-to-point and routed connections
  - Low-latency
  - High EMC, low power
  - High reliability
  - BER < 10-12

- SpaceWire extensions:
  - Protocol Identifier (PID)
    - Enables different protocols to operate concurrently over a SpW Network
  - Remote Memory Access Protocol (RMAP)
    - Configures SpW Networks and controls SpW nodes (read, write, rmw, acknowledged or not, security identification); RMAP has PID=1
SpaceWire Overview (1/2)

- Simple packet format

- Physical, Logical, Regional addressing

- SpW is event-triggered

- Time-codes allows time-triggered networks distributing system time

- Wormhole Routing

- Flow control avoids buffer overflow

- Group Adaptive Routing
SpaceWire Interface IP core

- Programmable TX speed from 5 to 100 Mb/s (5, 10, 50, 100)
- RX clock recovered from Data/Strobe
- Available with AMBA bus wrapper for stand-alone use
- Easy CAN connection by CAN-AHB bridge
- Easy connection to CAN bus by CAN-AHB IP bridge
- Parametric number of SpW interfaces plus a switching matrix
- Round robin arbitration policy
- Programmable router table
- Time codes for event and time triggered networks
- GALS approach for low power (internal clock generation)
- Status/control interface for error check and configurability
- SpW/AHB wrapper Master/Slave with DMA support and IRQ
- RMAP and PID HW support
- Test of the SpW Router integrated in the IPPM - Integrated Payload Processing and storage Module - board
- IPPM is an ESA space project with Aurelia spa and CAEN spa
- The IPPM board hosts our 8-port 100 Mbps SpW Router plus a 100 MHz ATMEL LEON2 CPU, several interfaces (CAN, MIL-STD 1553, UART, PCI mezzanine) and memories (FLASH, SRAM, PROM)
Code refinement phase:
SRAM-based FPGA (Altera Stratix II); lower development cost due to reprogrammability

Engineering model:
Antifuse FPGA (Actel AX); higher TID-tolerance (up to 300 krad), higher $T_j$ (up to 150°C), lower power consumption

Flight model:
Antifuse radiation-tolerant FPGA (Actel RTAX), with built-in SEU mitigation techniques (EDAC + scrubber, TMR)
- SEL immunity up to $LET_{TH} > 104$ MeV-cm$^2$/mg
- TMRed registers: SEU immunity up to $LET_{TH} > 37$ MeV-cm$^2$/mg
- Embedded SRAM with EDAC & scrubber: SEU rate $< 10^{-10}$ errors/bit-day
Target frequency

- **Problem**: 100 MHz target frequency and no availability of FPGA device with a high speed-grade (AX features speed-grade up to -3, RTAX only up to -1)
- **Solution**: Layout optimization through a manual custom floor-planning

- Region A: interfaces 1 & 2
- Region B: interfaces 3, 4, 5 & 6
- Region C: interfaces 7 & 8

The regions’ definition has been chained by the pin-out due to PCB layout constraints
SpW-Router complexity

- Router with 8 SpW interfaces + AHB and RMAP
  - ASIC complexity of 180 Kgates and 2.8 Kbytes RAM
  - Actel (RT)AX2000 -1
    - Speed: 100 Mbps TX, 200 Mbps RX
    - Area: 80% of available resources
    - Power: < 400 mW static, roughly 1 mW/Mbps dynamic
  - Altera Stratix II EP2S60
    - Speed: 200 Mbps TX and RX
    - Area: 25% of available resources

- Router with 4 SpW interfaces + AHB and RMAP
  - ASIC complexity of 125 Kgates and 2.2 Kbytes RAM
  - Same speed vs. the 8-port, Power consumption reduced by 30%
  - Fitted in smaller AX1000 and EP2S15 FPGAs
Prototyping Board

- Carrier Board: Nallatech BenNUEY-PCI
- On-board high-speed bus 122 bits@200MHz
- 3 SW programmable clock sources: 20 – 120MHz

**Xilinx Virtex-II XC2V8000**

**Nallatech PCI Adapter**

**PCI: 64 bits @ 66 MHz**

**I/O Module**
- **AHB bridge**: bridge for rapid prototyping of AHB IP cores (in-house development)
- Dedicated module for clock distribution and IP cores synchronization
- In the demo the router acts as a **loopback** on the PCI port
GUI at a glance

- Link control: activation & transmission speed
- Configurable real-time monitors for router links
- Host port (AHB) real-time monitor
- Hardware reset
- Single data transfer
- Multiple data transfer with path selection
- Activity log
Thank you!
Radiation effects in CMOS devices

- Long term cumulative effects: Total Ionizing Dose (TID)
  - Threshold voltage shift
  - Increased leakage current

- Single interaction effects: Single Event Effects (SEEs)

  Non-destructive:
  
  **Single Event Upset (SEU)**
  - Single bit errors in latches or memory elements

  **Single Event Transient (SET)**
  - Temporary change in logic output: system malfunction

  Destructive:

  **Single Event Latchup (SEL)**
  - Localized latchup due to parasitic thyristors

  **Single Event Gate Rupture (SEGR)**
  - Gate rupture of power transistors
Radiation mitigation at device level

- FPGA preferred to ASIC approach due to:
  - Lower non-recurring costs & development time
    Suitable for low-volume aerospace market & emerging phase in automotive scenario
  - Higher flexibility
    Suitable for the non-frozen standard

- Current commercial FPGAs show:
  - High TID tolerance
  - High SEL immunity
  - High SEU susceptibility (due to high density and geometry shrinking)
SRAM based FPGAs: Logic and routing configuration is hold in memory cells (reprogrammable FPGAs)

- Registers and memory cells need to be hardened
- Logic and routing sensitive to SEU

SEU mitigation techniques:

- Scrubbing: configuration memory readback and partial reconfiguration
- Error Detection And Correction (EDAC) techniques, usually for user memory: based on additional memory bits used to check for and possibly correct corrupted data
- Triple Module Redundancy (TMR): use of redundant hardware and voting circuitry
Antifuse FPGAs: Physical shorts between metal routing layers to configure logic (One Time Programmable)

- Logic and routing inherently insensitive to SEU
- Only registers and memory cells need to be hardened

SEU mitigation techniques:

- The same as for SRAM FPGAs, but need a reduced amount of additional resources (only for registers and memory cells)
- Radiation tolerant/hardened version of antifuse devices often provides built-in mitigation techniques (EDAC-enhanced memory cells with scrubber, registers with TMR)
Radiation mitigation at architectural level (1/3)

- Clock division
  The SpW Router has several clock domains. The TX clock and the internal routing clock are obtained by division of one input reference clock.
  - **Problem:** AX FPGA features PLL units but they are not available on RTAX-S
  - **Solution:** Implementation of digital clock dividers (prescalers) integrated in the radiation-tolerant logic of the antifuse FPGA

- TX/RX FIFO units
  Each SpW interface has a RX/TX FIFOs pair.
  - **Problem:** FIFOs on RTAX-S device are not SEE-tolerant
  - **Solution:** Custom FIFO made up of RAM EDAC blocks, available on-chip in the RTAX-S device, plus a proper controller, realized using radiation-tolerant logic → area occupation increased by 20%
Router and interfaces programming phase

- **Problem:** Loss of IPs control in case of malfunctioning of the programming mode
- **Solution:** Redundant programming access (via any of the 8 SpW links or via host bus); auto-flush procedure in case of programming errors

Packet exchange phase

- **Problem:** Possible link failure
- **Solution:** By means of Group Adaptive Routing (GAR), links are clustered as groups of at least two links, to implement path redundancy at network level. In case of a link failure, packets are routed through the other links belonging to the same group
Conclusions

- A complete set of IPs for a complex SpW Network set-up has been developed and fully tested in real systems accordingly to stringent ESA requirements.

- Radiation-mitigation issues have been addressed at both device-selection level and architectural level.

- The performances of the SpW IP cores meet the requirements of high-rate and fault-tolerant networks in avionics and space scenarios.